

****Gottlieb system80 Test Eprom V3.6 February 2018 by Marco Albus****

I wrote this test Eprom because after using Leon Borre's test Eprom many times I experienced problems with the reliability of the memory tests and the confusing indication from the results of the tests. After disassembling Leon's code my observations were confirmed and I decided to write a new test Eprom from scratch.

My goal was achieving more reliable test results for the memory chips present at the system 80 boards and a more clear indication/diagnosis for the several tests. Besides this I added a few bells and whistles and took a slightly different approach for a few things, maybe this will be a bit confusing for the people who are familiar with the test Eprom written by Leon Borré.

Preparations.

If your board is damaged by a leaking backup battery and this hasn't been cleaned up and repaired properly don't even start!

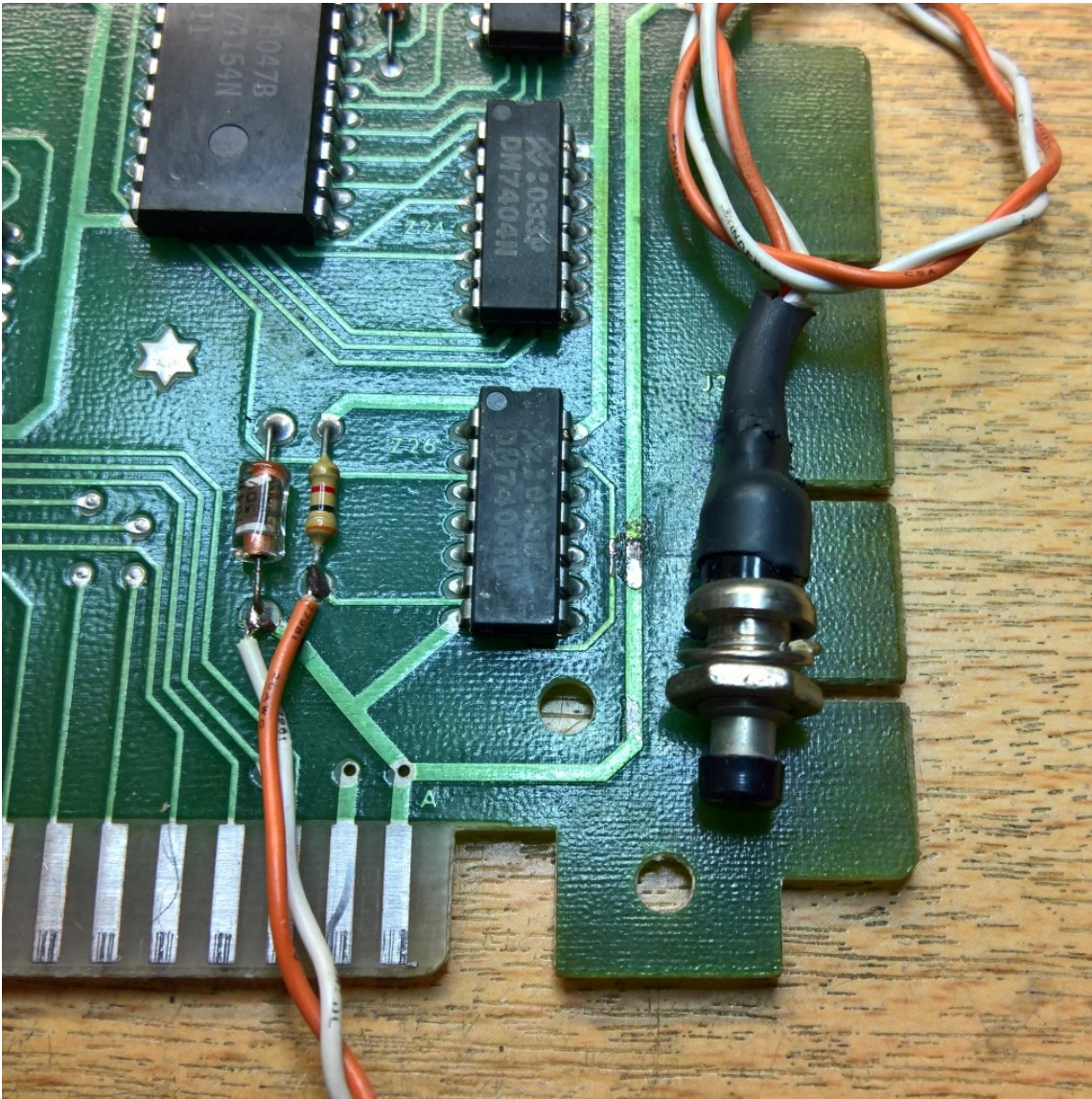
The testrom is intended to be used by people who are having skills in electronics and using solder irons. Despite the testrom will give you lots of information about your CPU board, the result will be dependable on your interpretation of this information and in the way your work is done at your board. This is also a disclaimer: I am not responsible for any failure in the repair of your CPU board. Having said all this: I really hope the testrom will route you to a successful repair and a fully functioning game again.

Further needs: for diagnosis an LED is necessary. This LED is connected between +5V and addressline a6 which is present at pin 15 of the 6502 processor. Use a 1K series resistor which prevents the LED from burning and prevents overloading the addressline. Microgrippers are a nice thing to have but you can also solder the LED temporary. If you have a Pinitech TC1 adapter or an aftermarket piggyback with an LED connected at addressline 6 you don't need to connect this extra LED for diagnosis.

The following test rom files are available:

- **SYS80_testEPROM1_2764.bin** Program this file in a 2764 Eprom. To be used for system 80B boards with piggyback or earlier system80 boards with an "aftermarket" piggyback. Install this test Eprom in socket at the piggyback installed in U3.
- **SYS80_testEPROM1_2x32.bin**. Program this file in a 2532 Eprom if you intend to use it in socket U3 at system 80 and system 80A boards. Program it in a 2732 Eprom if you are using the TC1 testadapter from www.pinitech.com. To be used for system 80 and system 80A boards in stead of masked ROM U3
- **Extended SYS80_testEPROM2_2716.bin**. Program this file in a 2716 Eprom. To be used in addition to testEPROM1 for system 80, system80A and system 80B boards which carry a 2716 gameROM in socket PROM1 (named socket PROM2 at system80B boards). This is an optional test Eprom for testing the PROM2 socket and the RIOT timers. It is not mandatory to use however. You cannot use testEPROM2 for older boards which carry 2 masked gameROM's Z38 and Z37 (PROM1 and PROM2).
- **Extended SYS80_testEPROM2_2732.bin**. Program this file in a 2732 Eprom. Additional test Eprom to be used in addition to testEPROM1 for testing the PROM2 socket at late system80B boards which use a 2732 PROM2 (Excalibur, Hot Shots, Bone Busters, Big House) and the RIOT timers. However, it is not mandatory to use.

If you are intending to use the Extended Testrom you need to connect a normally open, momentary pushbutton to the Slamswitch Input. If the Slamswitch modification has been performed at your CPU board, you will need to remove this temporary. You can reinstall it after testing again.

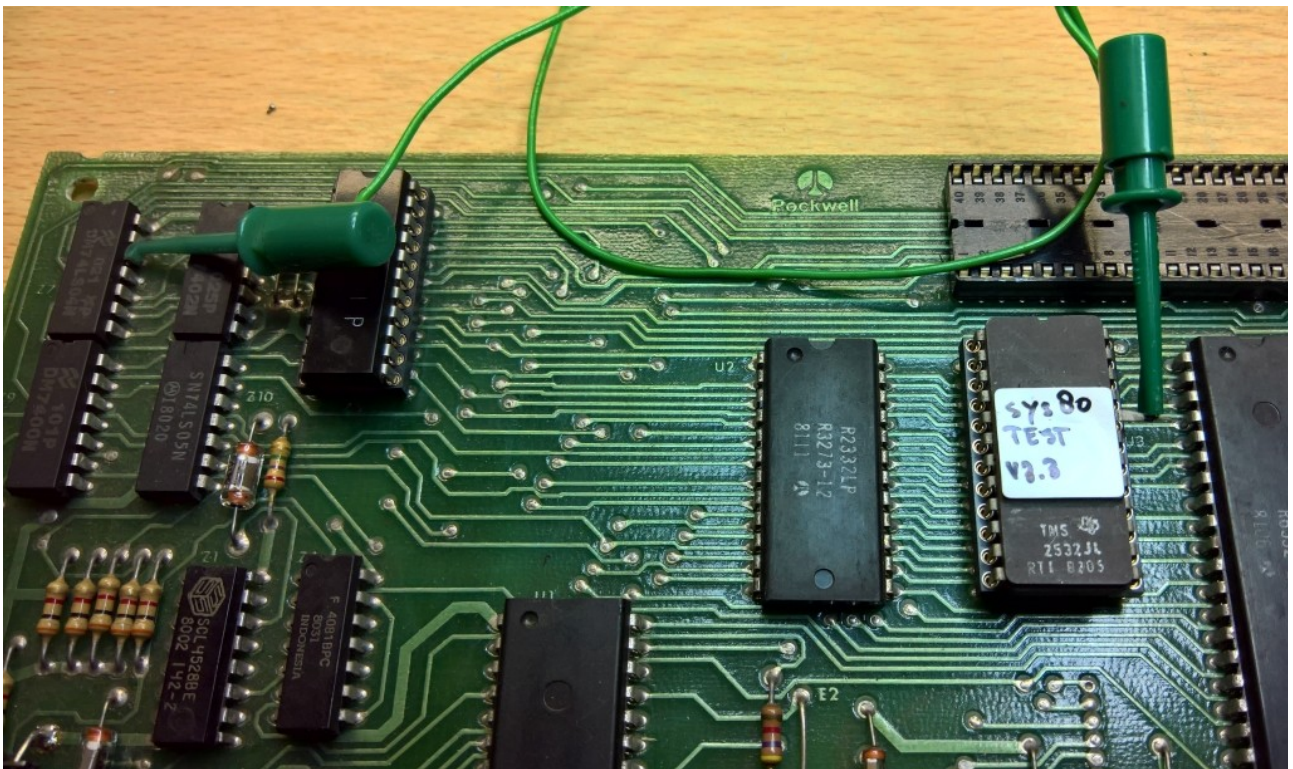


Connecting a pushbutton to the slamswitch input

Installing test Eprom1 for a system 80 board without piggyback.

For a system80 board you need to remove masked ROM U3 first. Since this one is most of the time directly soldered on the board you need to desolder this one first with proper desolder equipment and install a high quality IC socket in its place. Owners of a system 80A board are more lucky: most of the time the U2 and U3 masked ROM's are installed in IC sockets.

Technically, a 2532 Eprom differs from the U2 and U3 masked ROM's; so you cannot install the testEPROM1 directly into the U3 socket. You need to do the following: bend pin 20 from the 2532 testEPROM1 upwards and install it into the U3 IC socket. Now, connect PIN20 to addressline /a13 which is present at Z7 (7404) pin 12. Again, a wire with microgrippers is usefull but a temporary solder connection will do the job as well. Maybe it is a bit tricky to use the test Eprom like this but still it is a way more easy than Leon Borre's 2732 solution.



Using a 2532 Test Rom at U3

Installing the test Eprom in boards with (aftermarket)Piggyback

This is an easy one. You can install the 2764 testEPROM1 directly into the socket present at the piggyback. Some of the aftermarket piggybacks already have the a6 diagnostic LED installed.



Using the testrom in a -aftermarket- Piggyback

Installing the test Eprom in boards with a Pinitech(C) adapter installed at TC1

Pinitech provides a very nice tool which cooperates very nicely with the testrom. It has the a6 diagnostic LED already installed. The Pinitech adapter is to be installed in the TC1 socket. There is one thing you should be aware of when using the Pinitech adapter. The ROM installed at U3 (or piggyback in case of a system 80B board) should be removed or disabled in order to avoid conflicts between it and the testrom as they are using the same addressspace. And there can be only 1 program started at the same time. If you don't want to remove U3 you can disable it by grounding its selection signal. Do this by making a temporary connection between Z10 pin 6 (BAB13) and GND. This can be handy in case of system 80 boards where the U2 and U3 ROM's are not installed in IC sockets. For more information please browse to www.pinitech.com.



Pinitech TC1 testadapter

Installing extended test Eprom2

With extended testEprom2 you can test the PROM1 socket and the RIOT timers and allows you to test all the dipswitch banks and a connected driverboard during the I/O test. In system80B the same socket is named PROM2. It is used in addition to test Eprom 1. It is not mandatory to use Extended Test Eprom2. If it is not present the program in test Eprom1 just skips these tests. TestEprom1 already gives a lot of information about the board under test. For the first time testing a board I would recommend to use just testEprom1 and after that, testing the board more thoroughly with extended testEprom2.

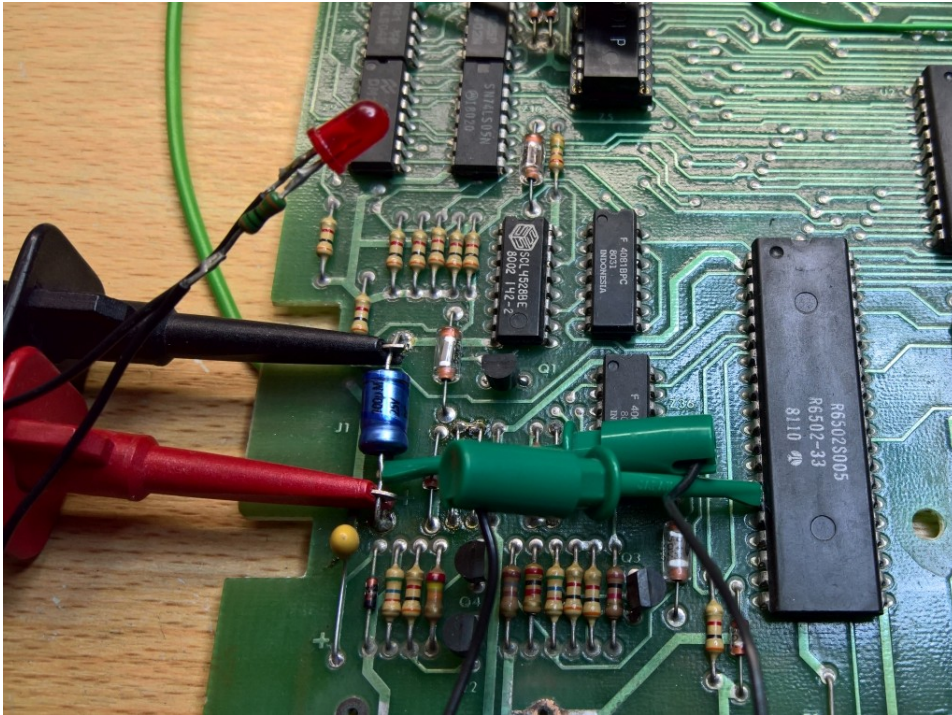
You can install test Eprom 2 directly into its socket. For late system 80B boards there is a 2732 version available, for earlier boards use the 2716 version. For boards still using 2 masked ROM's Z38 and Z37 (PROM1 and PROM2) it is not possible to test these sockets. If desired you can modify these boards for using a single 2716 Eprom.



Installing Extended testrom

Let's go.....start using the test Eprom!

A system 80 processor board can be powered up with a +5V DC single power supply. A system 80 board draws about 1 to 1.3 Amps, make sure your power supply can handle this. It makes sense to set the current limiter lower than 2 Amps to avoid burned traces as a result of a short circuit in one of the components, especially if you don't know the state of the board you are working on.



Connecting power and diagnosis LED to addressline a6

When a system 80 board is powered on with test Eprom's installed and a diagnosis LED connected a short flash will be seen as soon as the board is powered up. This short flash has to be ignored. After this a sequence of flashes will be seen (if the board is okay) as described below:

1 long flash

After a few seconds a long flash is indicated by the diagnosis LED connected at a6. This tells us the test Eprom is running. The 6502 CPU is okay, the selection circuitry for the U3 socket is okay, the reset section appears to be okay, same for the clock circuitry. Pay attention now, after the long flash appeared, the following flashes will be a bit more fast. If the LED is stuck on or the long flash doesn't appear check the following:

- Reset circuitry. Pin 40 of the 6502 processor should be 5 Volts.
- Clock circuitry. Is the clock signal present at pin 37? Is clockbuffer Z3 a 7404 and NOT an LS04, HCT04, S04,
- Is the 6502 processor ok?
- Check traces, especially when the board suffered from a leaking battery or someone has been working on the board before.
- Another defective chip may cause a jammed address or databus line. Remove the 5101, U2 and the 3 RIOT's. If the long flash appears now, reinstall the removed chips 1 by 1 to determine which chip is defective.
- Selection circuitry for the U3 socket and addressbuffers Z7, Z8, Z9, Z10, Z12

1 short flash.

The 5101 memory has been tested for 5 times with different patterns over its whole range and is okay. Please note the short flash is preceded by a shorter faint flash. This is caused by writing and reading the memory over its whole range which affects addressline a6. The same can be said about the memory tests for the RIOT's which will follow afterwards.

If the short flash doesn't appear and the test program stalls check the following:

- The 5101 chip itself.
- Traces between the 6502 and 5101 and its selection circuitry. A must do if someone has been working on the board before or the board was affected in the past by a leaking battery.
- The 6502 processor. The R/W line of the 6502 processor can be defective. Earlier boards didn't have a 3K pull up resistor at the R/W line to prevent it from overloading. Gottlieb added a pull up resistor later which was installed at the TC1 adapter to the reset circuitboard. It is a good idea if this resistor is not present to add one at the solder side of the board.
- The selection circuitry Z4 and Z36.

Note: the 5101 chip is only used for bookkeeping en highscores. If the chip is not installed the board will power up normally with regular game ROM's.

A burst of 2 short flashes

The memory in the switchmatrix RIOT U4 has been tested and is okay.

If the 2 flashes don't appear check the following:

- Clock signal at pin 39 of the 6532 RIOT's. If it is not present check the Z3 clockbuffer and the traces around the clockbuffer as they are often affected by corrosion due to a leaking battery.
- The 6532 RIOT itself. This one is often failing due to short circuit problems in the switch matrix under the playfield (someone tried to adjust an EOS or popbumperswitch while the machine was powered on and made a short between the switchmatrix and a solenoid line.....). Often one or more of the switch matrix buffers Z11 ~ Z15 is or are failing too.
- The selection circuitry Z7 and Z8.

Note: the memory range covered by RIOT U4 is used as "zeropage memory" by the 6502 CPU. In this range a program stores its variables, registers, temporary data.....

A burst of 3 flashes

The memory in display RIOT U5 has been tested and is okay.

Check the RIOT itself and its selection circuitry if the test is failing. Something about the RIOT test: in theory it is possible the test is writing and reading a different RIOT as desired due to stuck selection circuitry for the RIOT's. The test program writes unique ID's to each RIOT and reads it back before testing its memory. If the desired ID is not read back the test will stall.

Note: the memory in RIOT U5 covers the second part of the zeropage for the 6502 CPU.

A burst of 4 flashes

The memory in Solenoid/Lamp RIOT U6 has been tested and is okay.

Check the RIOT itself and its selection circuitry if the test is failing.

Note: the memory in RIOT U6 covers the stack for the 6502 CPU. The stack is used to store the program counter and registers when calling subroutines or Interrupt routines.

THE NEXT TESTS ARE ONLY EXECUTED IF EXTENDED TESTPROM2 IS PRESENT

Note: as said before, when testing a board for the first time I would recommend to test it first with testEprom1 only which already provide you lots of information about the board you are testing. Afterwards, you can test it more thoroughly with extended testEprom2.

If extended test Eprom is not present, the socket and Timer tests are skipped and the testprogram will execute the I/O tests for the RIOT's.

A burst of 5 flashes.

Socket PROM1 (PROM2 at system 80B boards) is okay as are the signals (address- and databus, selection) running to the socket.

Check the following if the test fails:

- Traces from 6502 CPU to socket PROM2 and selection circuitry
- Selectioncircuitry and addresslinebuffers Z7, Z9, Z10, Z12.
- If the board is modified for using a 2716 at PROM2 in stead of the 2 masked ROM's S1 and S2, check the modification
- If working on a newer board check if the board is properly jumpered (E3, E4,). When using the 2732 PROM2 check if addressline a15 is present at socket PROM2 coming from socket TC1 pin 35. If not, you can jumper your board in an alternative way to accommodate a 2732 PROM2:
 - remove jumpers E3 and E4
 - solder a wire from socket TC1 pin 35 to the point where E3 and E4 meet. There is no need to cut any traces when using this method.

The RIOT Timer Interrupt tests will follow now.....observe the addressline LED!

A long flash followed by a short flash.

All Timers in switchmatrix RIOT U4 generated 4 interrupts each which were processed properly.

A long flash followed by a burst of 2 short flashes.

All Timers in display RIOT U5 generated 4 interrupts each which were processed properly.

A long flash followed by a burst of 3 short flashes.

All Timers in lamp/solenoid RIOT U6 generated 4 interrupts each which were processed properly.

The testprogram will stall if one of the “extended tests” fail. Otherwise, it will continue and execute the I/O tests for the RIOT's.

INPUT / OUTPUT TEST 6532 RIOT's.

Now the memories have been tested the testprogram jumps over to its final test: testing the inputs and outputs from the RIOT's U4, U5 and U6. For those who are familiar with Leon Borre's test Eprom something has changed here. Leon used to program all I/O lines from the RIOT's as outputs regardless the boards design. Some outputs are fighting outputs here. By the system 80 design, some RIOT I/O lines are used as being Inputs and others as being Outputs and this is the way this test Eprom is programmed. Goal of these tests is to find out if the RIOT's ports and the connected components are able to make "0" to "1" transitions and the other way around.

Each RIOT has 2 I/O ports A and B. Each port has 8 I/O lines:

PORT A PA0 ~ PA7 is situated at pins 8 ~ 15

PORT B PB0 ~ PB7 is situated at pins 24 ~ 16

Pin 20 is connected to +5V.

I/O test RIOT U6 - solenoid/lamps/sound

Let's start testing U6 first. Both I/O ports A and B are completely programmed to be outputs. During the I/O test all the outputs are pulsing between 0 and 5 volts. If an output does not pulse it can be defective and the RIOT has to be replaced. But another cause can be a defective input port from a component driven by the output which jams the output. Removing this component should bring the output back to live, if not replace the RIOT.

Oversight of Port A RIOT U6 and its behavior during the I/O test

PA0 ~ PA3: data for solenoid selector 74LS139. These outputs are pulsing slowly with half the frequency of the LED connected to A6. These outputs also drive the 7408 AND gates which are telling the soundboard which sound(effect) to play. All outputs should pulse but this time not in synch with the a6 connected LED.

PA4. Output which drives a 7404 buffer and the 7408 sound selector. Should pulse in synch with the a6 connected LED.

PA5 ~ PA6: these outputs are enabling the multiplexers in solenoid selector 74LS139. The outputs are pulsing fast, with double the frequency of the LED connected to addressline a6. The 74LS139 is driving the 2 7416 buffer chips which are feeding the power transistors at the driverboard. The outputs of the 74LS139 selector and 7416 buffers should pulse one time every 2 flashes of the LED connected to a6. Since version 3.4 of the testrom, these outputs are all active.

PA7. Output which will be pulsing in synch with the a6 LED. Drives a 7416 gate which should pulse in the same manner.

Oversight of Port B RIOT U6 and its behavior during the I/O test.

PB0 ~ PB3. Outputs driving 7417 buffers. These provide the 74175 latches at the driverboard with data. All these should be pulsing in slowly, with half the frequency of the a6 connected LED.

PB4 ~ PB7: data for the 74175 latch and dipswitch bank selector 74154 (Z33). PB0 ~ PB3 should be pulsing in synch with the a6 connected LED. Z33 74154 selects dipswitch bank 1 during the I/O test. If you are using the Extended Testrom, you can select during the I/O test dipswitch bank 1 to 4 or 1 of the outputs from the 74154 multiplexer which selects at at driverboard - if connected – a 74175 latch. This test is described later on.

I/O test RIOT U5 - Display/slamswitch input/DIP switch enabling

For RIOT U5 PORT B PB7 ~ PB0 are all outputs. Same for PORT A PA6 ~ PA0. PA7 is an input for the slamswitch. In Game mode, if this input is activated, the program will be restarted and your game will be lost.

Oversight of Port A RIOT U5 and its behavior during the I/O test

PA0 ~ PA3. These outputs are controlling digit selector Z25, 74154. Since testrom V3.5 these outputs are sending a data pattern to the 74154 digit selector. All the outputs are pulsing but not necessarily in synch with the a6 connected LED. With an oscilloscope you can observe the 74154 outputs and the 7404 inverters which are connected to these outputs. Every once in a while they should pulse.

PA4 ~ PA6. These outputs are now pulsing with double the frequency of the a6 connected LED. These signals are clocking the 74175 latches connected to port B from RIOT U5.

PA7. Slam input buffered by a 7404 inverter gate. You can investigate the behavior of the Inverter gate by simply connecting the input to GND.

Oversight of Port B RIOT U5 and its behavior during the I/O test

PB3 ~ PB0. These outputs are providing the 74175 latches with data. In system 80 and system 80A the latches are connected to the 7448 7 segment decoders. On system 80B boards, these 7448 chips are not used. From testrom V3.4 and on, you can investigate the 74175 and 7448 outputs if installed. Especially, the 7448 are failing sometimes after someone removed a connector while the game is powered on. The PB3 ~ PB0 RIOT outputs will all pulse but not necessarily in synch with the a6 connected LED.

PB4 ~ PB6. These outputs are driving 7404 inverter gates. All these are pulsing in synch with the a6 connected LED.

PB7. These signal is enabling the dipswitch banks. It should pulse during the I/O test in synch with the a6 connected LED. Investigate also the inverter between the RIOT's output and 7432 OR gates.

I/O test RIOT U4 - Switch Matrix Control

RIOT U4 is taking care of the switch matrix in system 80 games. It is an important one to test because this one is many times defective due to a problem under the playfield (a loose wire touching the coil voltage) or due to a user error (adjusting a switch under the playfield while the game is powered on).

Port B PB7 ~ PB0 are all outputs and are driving 7404 inverter buffers. Port A PA7 ~ PA0 are all inputs and are buffered by Z13 and Z14 (both 7400). Each buffer has 2 inputs: 1 for the DIP switches and 1 for the switch matrix, this allows the RIOT to read the DIP switches *or* the switchmatrix.

Let's test the DIP switches first. Initially, the first dipswitch bank (1 ~ 8) should be active. Since testrom V3.6, with the Extended Testrom, you can select Bank 2, 3 and 4 as well. This will be described later on.

Set all DIP switches 1 ~ 32 to “OFF” position. In this condition PORT B, all PB7 ~ PB0 should stay static at 0 volts. If a port is pulsing there is probably a NAND buffer in Z13 or Z14 defective. Use an Oscilloscope or Logic Probe to determine which port at Z13 or Z14 is defective. It is not unfamiliar for these ports to be defective as they are often blown up by a short circuit in the switchmatrix under the playfield.

Now, set all dipswitches *other than the active dipswitchbank* to “ON” position. In this condition, all outputs at PORT B should not be influenced and remain static at 0 Volts. If one of these switches cause an output to pulse check Z33 (74154) and Z15 (7432). These chips take care of which dipswitchbank is selected. There should be only 1 selected at the time.

If all the outputs from PORT B stay static at 0 volts set DIP switch 1 to “ON” position. This alters via a NAND buffer RIOT's input PA7. Now, PB7 at PORT B should start pulsing now. If DIP switch 2 is set to “ON” position, input PA6 will be altered and PB6 should start pulsing in synch with the a6 connected LED. Output PB5 will do the same for DIP switch 3 (alters PA5) and so on. Don't forget to check the 7404 Inverter gates connected to the outputs which are driving the switch matrix. Not seldom, these are fried after a short in the switchmatrix.

When an output is not responding to a switch check the following:

- The DIP switches themselves. Often they not work properly anymore due to age or due to a battery which has been leaking in the past.
- An output can be jammed by a defective port in Z11 or Z12. Your finger can be an aid for finding a defective chip. Touch Z11 ~ Z15. If you burn your finger at one replace it ;-) You can remove outputbuffer Z11 without a problem to check if this one jams one or more outputs. Z12 is used on later boards also as an addresslinebuffer; the CPU board doesn't run without it.
- Inputbuffers Z13 and Z14. Use an Oscilloscope or Logic Probe
- DIP switch enable buffers Z15 (7432) and dipswitch bank selector Z33 (74154)
- The RIOT itself

When the DIP switch circuitry is working properly you can test the Switch Matrix input. Set all DIP switches 1 ~ 8 to “OFF” position. Observe the RC networks R12 ~ R19 / C16 ~ C23 above the DIP switches. Short C16 with a wire with microgrippers. PB0 should go pulsing now. If C17 is shorted, PB1 should go pulsing. PB2 should go pulsing if C18 is shorted and so on. If an output does not respond the corresponding inputbuffer at Z13 or Z14 is probably defective.

<i>PORT A</i>	<i>RIOT pin</i>	<i>Input buffer</i>	<i>PORT B</i>	<i>RIOT pin</i>	<i>Output buffer</i>
PA0	8	Z13 pin 11	PB0	24	Z12 pin 1
PA1	9	Z13 pin 8	PB1	23	Z12 pin 3
PA2	10	Z13 pin 3	PB2	22	Z11 pin 13
PA3	11	Z13 pin 6	PB3	21	Z11 pin 11
PA4	12	Z14 pin 11	PB4	19	Z11 pin 5
PA5	13	Z14 pin 8	PB5	18	Z11 pin 3
PA6	14	Z14 pin 3	PB6	17	Z11 pin 1
PA7	15	Z14 pin 6	PB7	16	Z11 pin 9

Remark: a switchmatrix short not only fires the switchmatrix buffers and RIOT U4 but also the diodes used in the switchmatrix. Gottlieb applied Germanium diodes which have a low $V_{forward}$ to meet the logic levels as good as possible. A disadvantage here is that Germanium diodes are vulnerable for abuse and are often blown after a switchmatrix problem. It is a good idea to check them. It is recommended to replace them with Germanium diodes again (1N270, AA118,) or a schottky diode (BAT46, BAT85,).

Additional I/O test when using Extended Testrom V3.6 and later

Extended Testrom V3.6 and later adds a few features to the I/O test and even allows you to test a driverboard to the max.

As said before, it is recommended to test your system 80 CPU board first without the Extended testrom. When your board is succeeding all the “basic” tests, the time has come to test your board with the additional Extended Testrom. This Extended testrom will test, as described earlier, all the RIOT’s internal Timers before ending up in the I/O test.

The extended Testrom now controls the selected output from 74154 selector Z33. This chips selects one of the dipswitch banks or, via 7404 Inverter Gates at the CPU board, a 74175 latch at the driverboard. Now the momentary pushbutton which is connected to the Slamswitch Input comes into action. Initially, the first and the last outputs from Z33 are active during the I/O test. Z33 has 16 outputs. The first output selects dipswitch bank 1 which we tested earlier. The last is unused but pulsing anyway.

Now press the momentary pushbutton briefly. You will notice 3 fast flashes at the a6 connected LED. If you are not getting the 3 fast flashes, investigate the Inverters in Z26, pin 13 and 12. Or remove a slamswitch mod if it is still installed. Pressing the pushbutton generates an Interrupt. It is doing this in real life too, but then your game will reset and you will lose your game if you were playing one a little bit rough. This Interrupt is indicated by the 3 flashes. Also the data for the 74154 selector Z33 is updated and the program will return to the regular I/O test. The a6 connected LED will continue its flashing like it did before pressing the pushbutton.

As a result of this action dipswitch bank 2 is selected. Now you can test dipswitch bank 2 in the same way as you tested bank 1 before. Another press of the button will select dipswitch bank 3, and again another press, dipswitch bank 4. After 8 times pressing the pushbutton, dipswitch bank number 1 will be selected again.

Now, you can connect a driverboard also if you would like to test it in conjunction with the CPU board. The driverboard will be supplied by the CPU board, there is no need to add extra power wiring. You can now follow the signals from the 7408 AND sound control gates (Z31) at the CPU board to the outputs from the inverter gates at the driverboard, Z13 (7404).

You can also follow the signals from the 7416 gates at the CPU board (Z29, 30) to the powertransistors at the driverboard. At the base of each transistor, you should recognize the same signal. A transistor can still be defective though, check these with your multimeter.

We can also check the outputs from the 74175 latches. Initially, none of the latches are active, just dipswitch bank 1 is, at the CPU board. Now press the pushbutton again, connected to the slamswitch input. You will introduce an Interrupt, as a result the a6 connected LED will flash 3 times and will go back to normal again. Now, the 2nd output from Z33 will make dipswitch bank 2 active and also latch Z1 (74175) at the driverboard via signal DS1. This signal is clocking the latch. The latch will now copy the contents at the inputs to its outputs. The input signals are coming from 7417 buffer chip Z32 at the CPU board. You will see outputs at pins 2, 7, 10 and 15 from latch Z1 pulsing in the same slow frequency as those at the 7417 buffer chip (half the a6 LED's frequency).

Another press of the button will activate the next dipswitch bank and via signal DS2, latch Z2. Latch Z1 will be at ease again. Again you can investigate the latches' outputs. Another press will activate Z3 but also Z12., Then Z4 and Z11. After 8 times pressing the button, the test is again at its initial position. Table below clarifies the whole sequence.

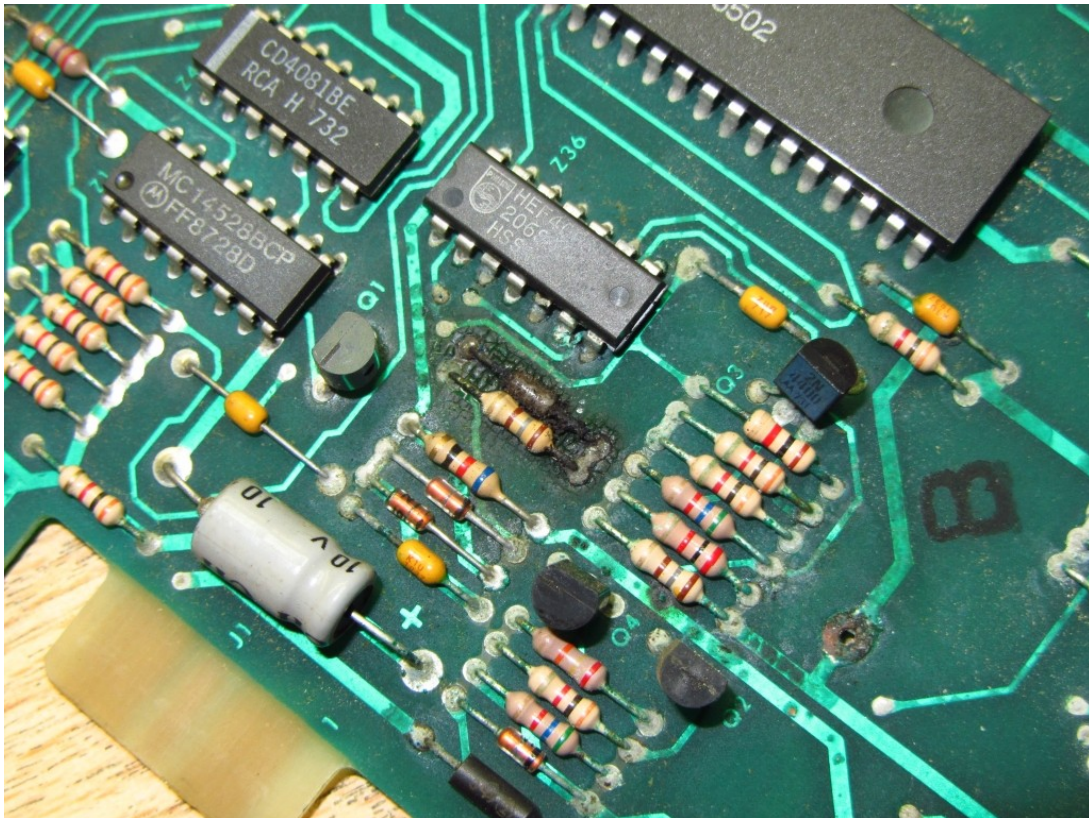
State ↔ pressing button	Dipswitch bank active	Latches active driverboard
1 (initial)	1 (1-8)	-
2 (after first button pressing)	2 (9-16)	Z1
3	3 (17-24)	Z2
4	4 (25-32)	Z3, Z12
5	-	Z4, Z11
6	-	Z5, Z10
7	-	Z6, Z9
8	-	Z7, Z8

This will end the testing of your CPU board and driverboard if connected.

Reset circuit modification

After repairing many many Gottlieb system 80 processor boards I noticed the 3 Volts zenerdiode VR1 is burnt often. A close look in the schematics tells why. There is a design error in the undervoltage protection circuit.

Zenerdiode VR1 applies a 3 volts reference voltage to the base of PNP transistor Q1 (MPSA70). The emitter from this transistor is fed by 5 volt minus a 0.6V voltage over diode CR35 = 4.4V. As a result the transistor will open. The Ueb characteristic of an opened transistor will be around 0.6V. So, at the base there will be $4.4 - 0.6 = 3.8V$. But.....as we saw earlier, VR1 tries to apply a 3V voltage to the base. The zenerdiode and transistor are now fighting with each other. Often, VR1 looks dark or worse and sometimes Q1 is damaged as well.



A simple solution to prevent VR1 from burning is the following:

- 1) replace VR1 (3V zener 500mW) and Q1 (MPSA70, 2N4403)
- 2) At the solder side of the PCB, cut the trace running from the base of Q1 to the VIA or plated hole.
- 3) Solder a 1K5 resistor over the base from Q1 and the VIA. An extra resistor is now added in series to the base from VR1. This resistor is low enough to drive Q1 into saturation and handles the potential difference. Now Q1 and VR1 stay healthy.

